Amendments to the Claims:

This listing of claims replaces all prior versions.

Claim 1 (currently amended): A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films for blocking penetration of moisture, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane parallel to said substrate, a conductive wall filling said groove in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface of said substrate when viewed in a direction perpendicular to said principal surface of said substrate,

and wherein said interlayer insulation films comprise a first insulation film that supports said conductive wall laterally and a second insulation film that supports said conductive pattern laterally,

said conductive wall and conductive pattern comprising Cu,

said conductive pattern and said second insulation film having coplanar top principal surfaces,

a bottom edge of said conductive wall making an intimate contact with said top principal surface of said conductive pattern, and

said conductive pattern and said second insulation film located at a top part of said multilayer interconnection structure being covered continuously with an insulation film.

Claim 2 (original): A semiconductor device as claimed in claim 1, wherein said guard ring pattern extends continuously along said periphery of said substrate.

Claim 3 (original): A semiconductor device as claimed in claim 1, wherein said conductive pattern extends in the form of a straight line along a peripheral edge of said substrate.

Claim 4 (original): A semiconductor device as claimed in claim 1, wherein said conductive pattern changes a direction thereof repeatedly and alternately in said plane in correspondence to said conductive wall.

Claims 5 and 6 (canceled)

Claim 7 (previously presented): A semiconductor device as claimed in claim 1, further comprising an etching stopper layer interposed between said first insulation film and said second insulation film.

Claim 8 (withdrawn): A method of fabricating a semiconductor device, comprising the steps of:

depositing an interlayer insulation film on a substrate;

forming a first groove in said interlayer insulation film to as to extend continuously along a periphery of said substrate;

forming a second groove in said interlayer insulation film such that said second groove extend continuously in said first groove;

depositing a conductive layer on said interlayer insulation film so as to fill said first and second grooves; and

removing a part of said conductive layer locating above said interlayer insulation film by a chemical mechanical polishing process, to form a guard ring pattern filling said first and second grooves,

wherein said step of forming said second groove is conducted such that said second groove changes, in said first groove, a direction thereof alternately and repeatedly in a plane parallel to said substrate.

Claim 9 (withdrawn): A method as claimed in claim 8, wherein said step of forming said first groove is conducted such that said first groove extends in a straight pattern along a peripheral edge of said substrate.

Claim 10 (withdrawn): A method as claimed in claim 8, wherein said step of forming said first groove is conducted that said first groove changes a direction thereof alternately and repeatedly in said plane in correspondence to said second groove.

Claim 11 (withdrawn): A method as claimed in claim 8, wherein said conductive layer is formed of Cu.

Claim 12 (withdrawn): A method as claimed in claim 8, wherein said step of forming said interlayer insulation film comprises the steps of: depositing a first insulation film on said substrate; depositing an etching stopper layer on said first insulation film; and depositing a second insulation film on said etching stopper layer, said step of forming said first groove comprises the step of: etching said first insulation film until said etching stopper layer is exposed, and wherein said step of forming said second groove comprises the step of etching said etching stopper layer and said second insulation film until said second groove reaches a bottom principal surface of said second insulation film.